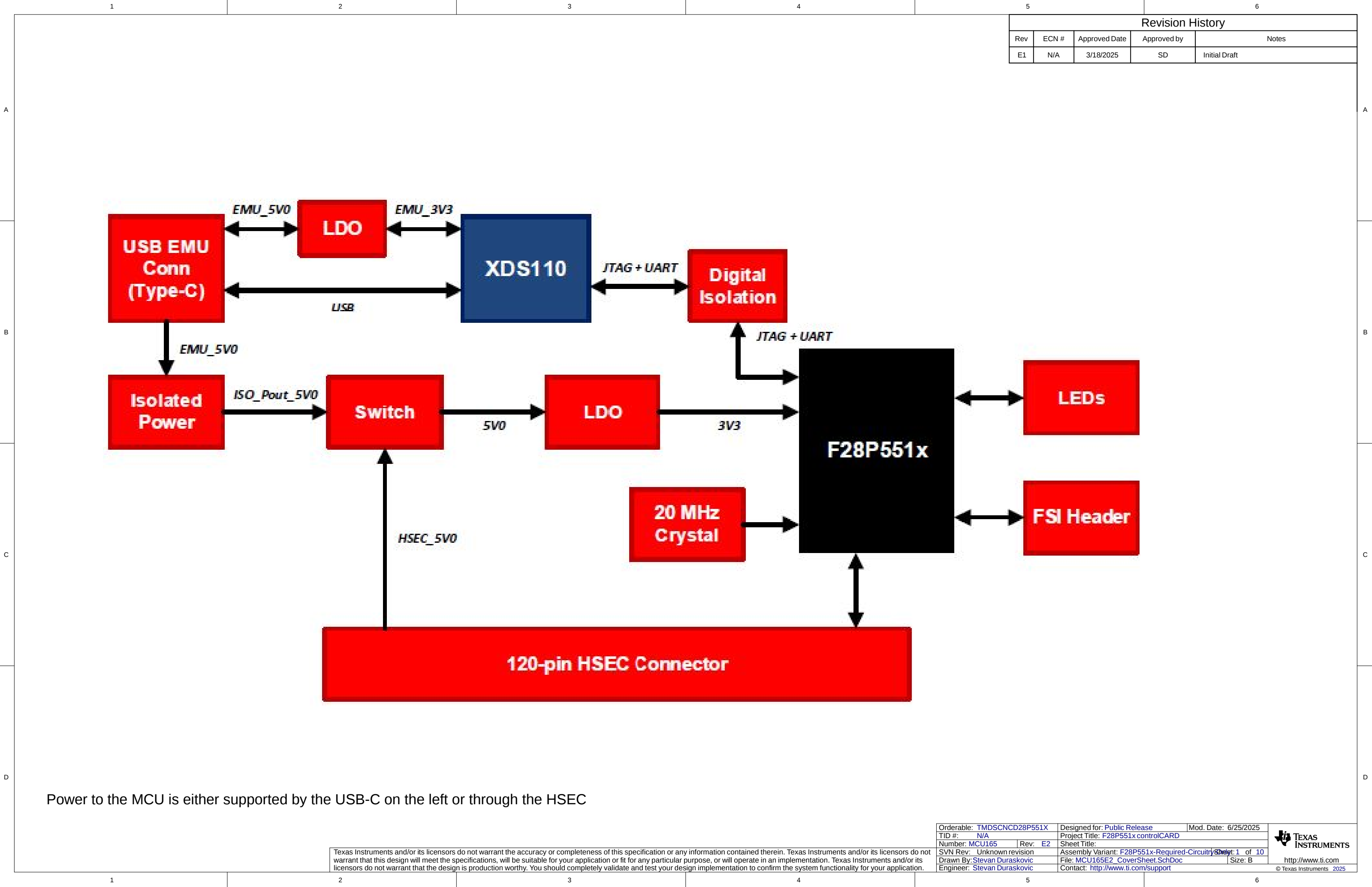
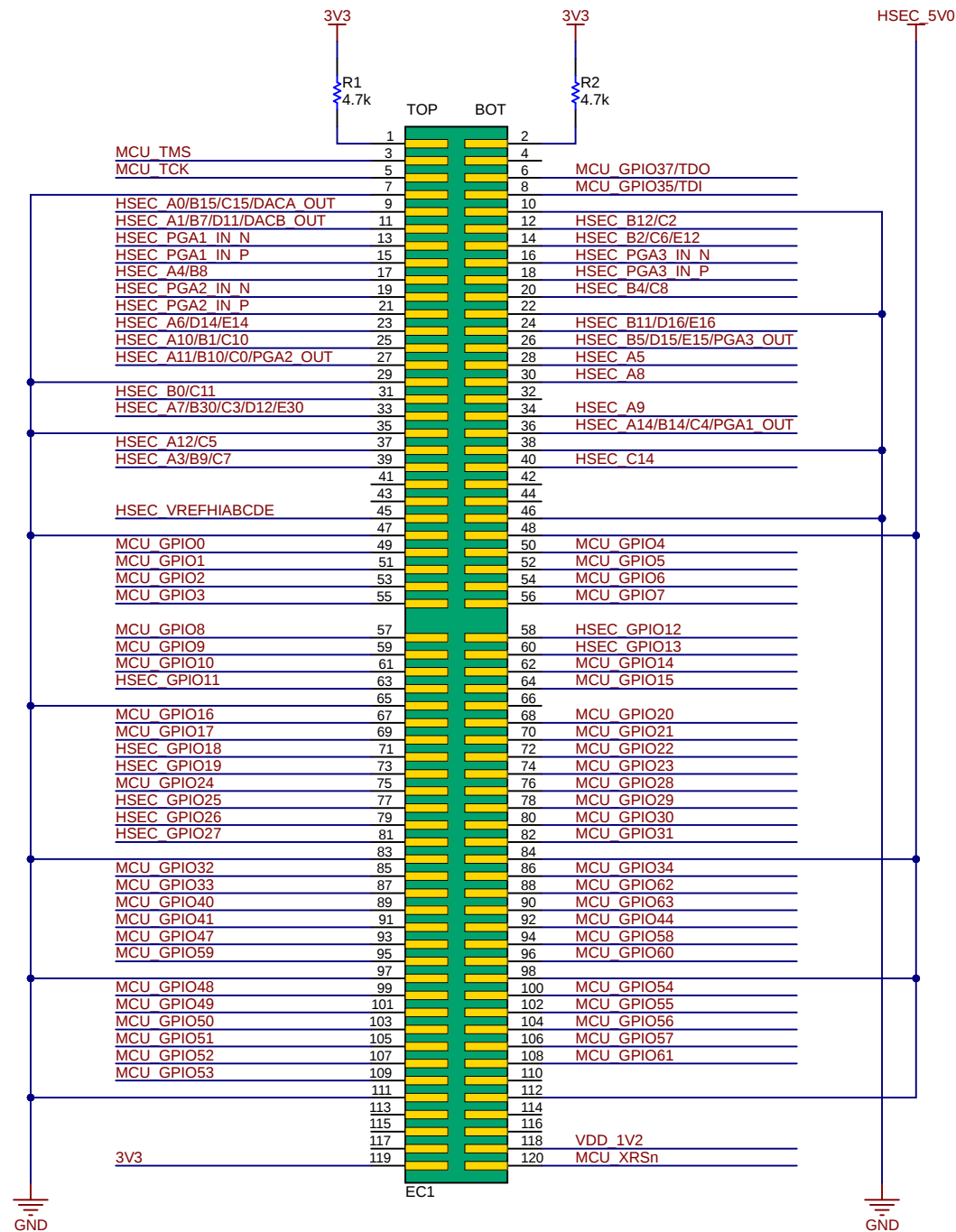
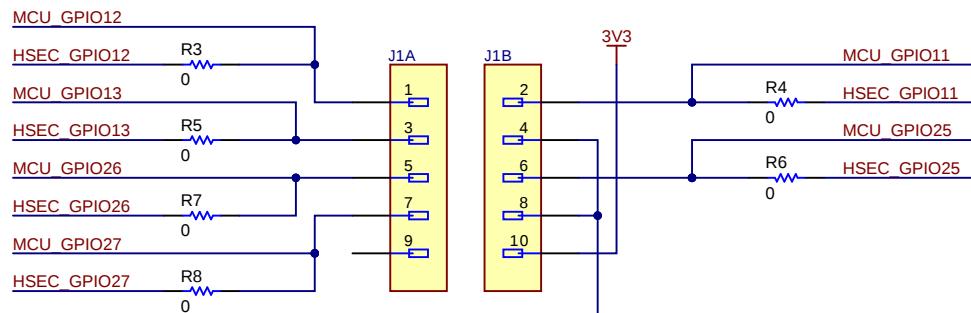




J1 has been updated over previous designs. Pins 9 and 10 were added enabling power to the connector. Additionally Pins 2 and 6, previously GND, have been repurposed to enable the full 3 pin FSI communication. The user can shunt HSEC GPIO11 and HSEC GPIO25 to ground if backwards compatibility is required.

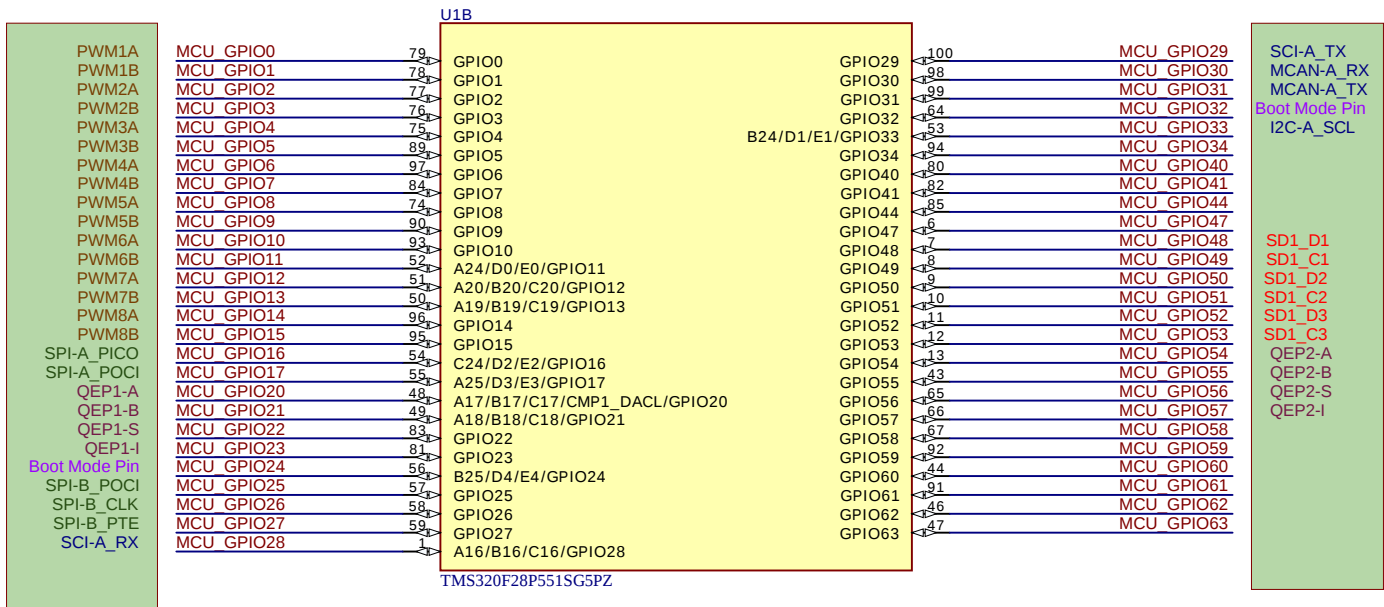


10-pin FSI Connector



1	FSI-RX0	2	FSI-RX1/GND
3	FSI-RXCLK	4	GND
5	FSI-TX0	6	FSI-TX1/GND
7	FSI-TXCLK	8	GND
9	KEY	10	3V3

Pin 9 of J1 is cutoff to key the connector

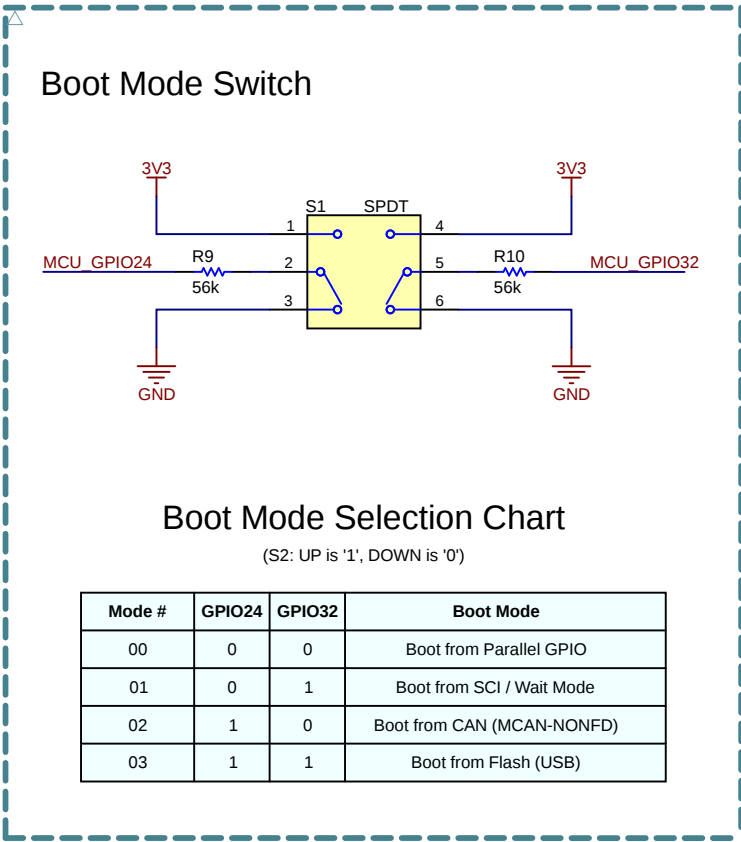
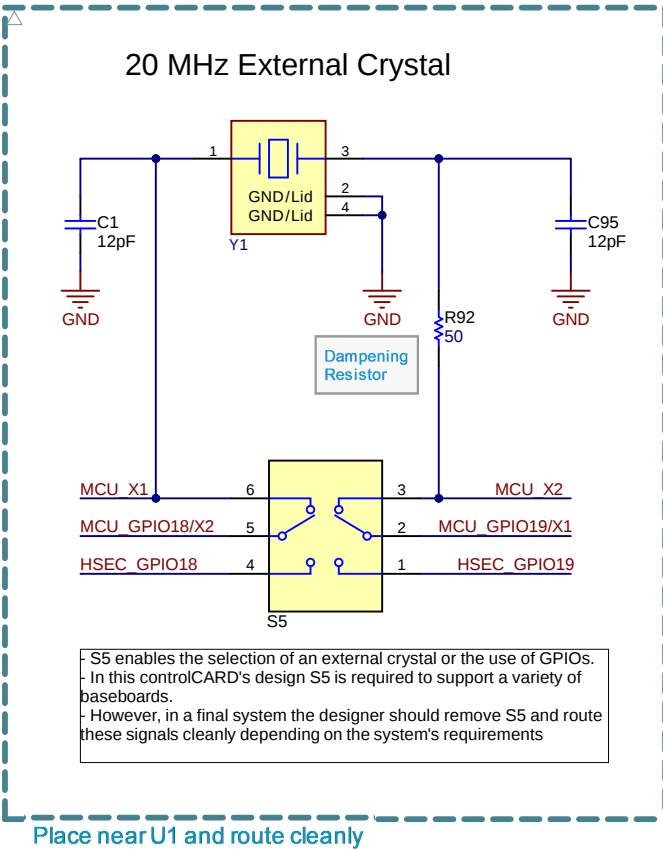
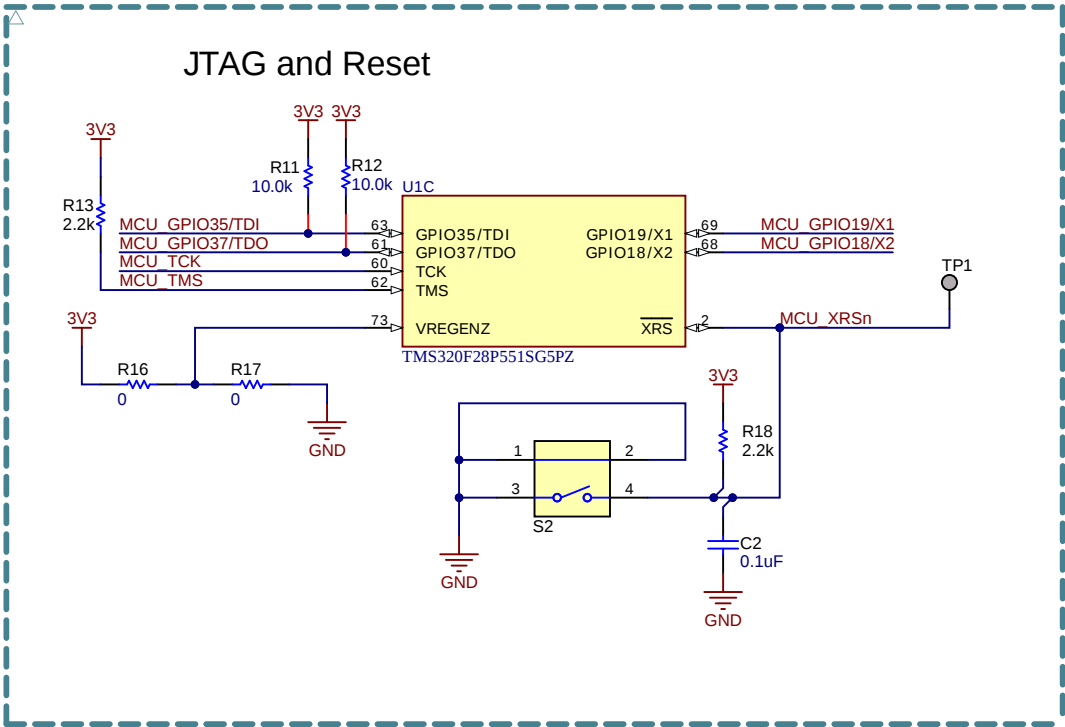


A

B

A

B

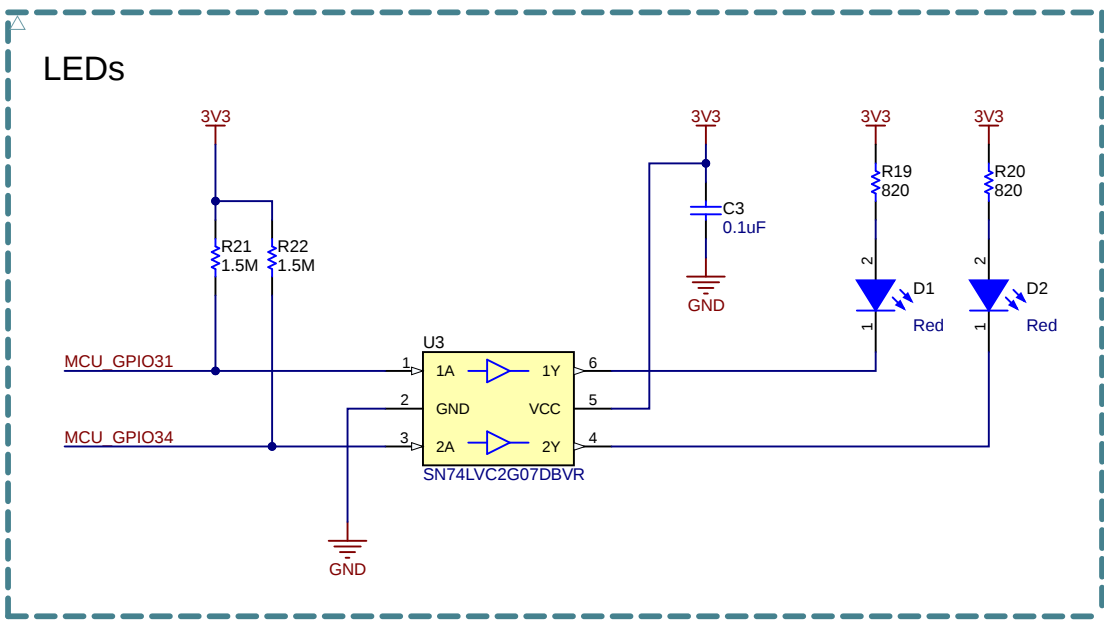
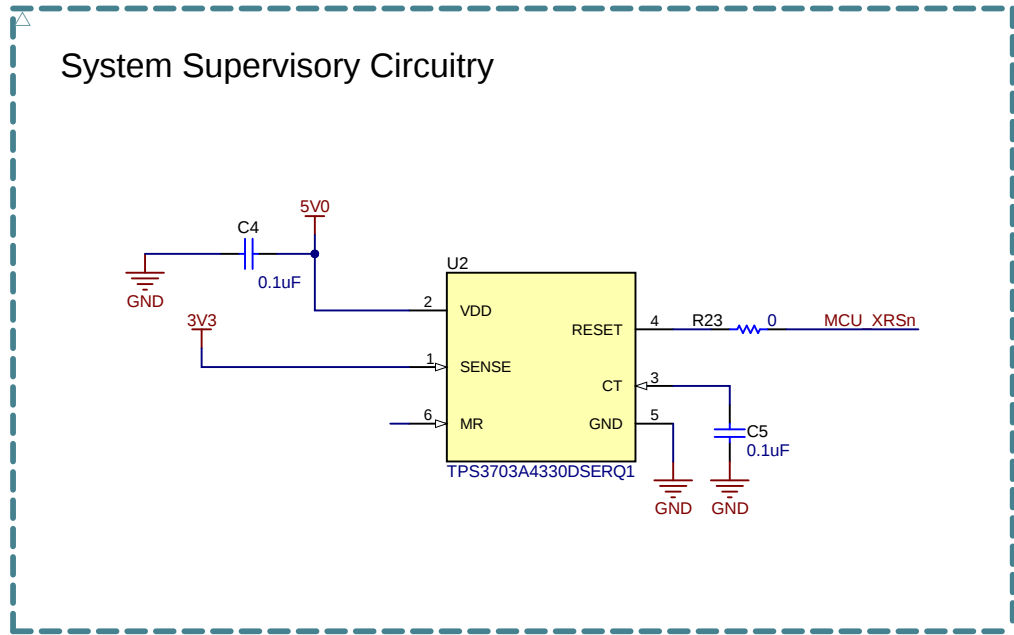


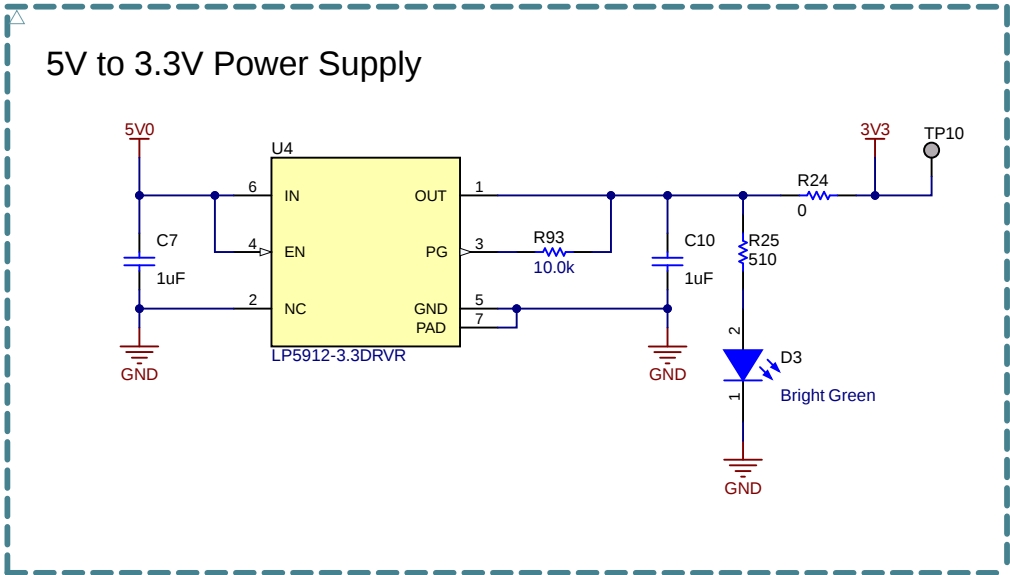
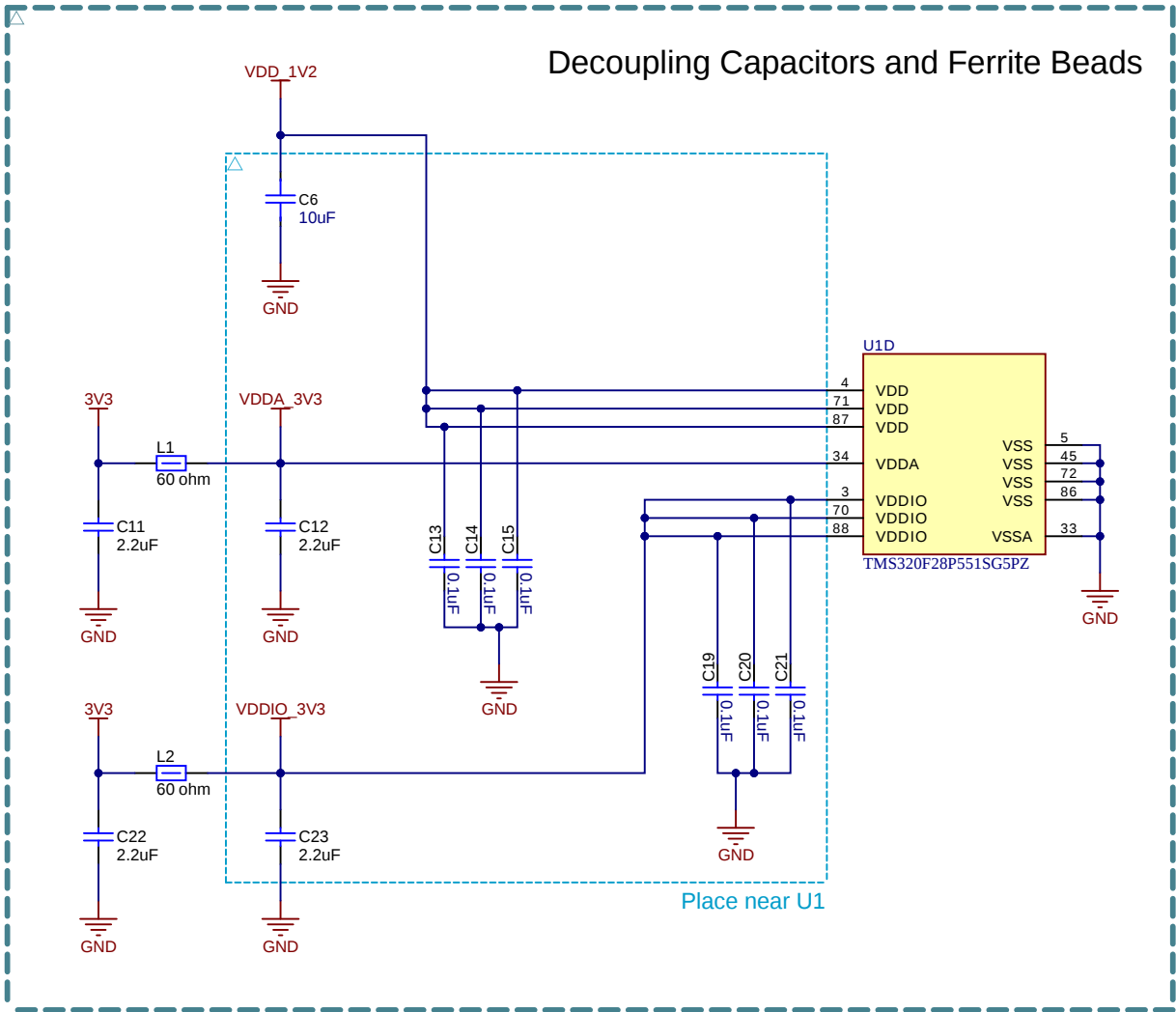
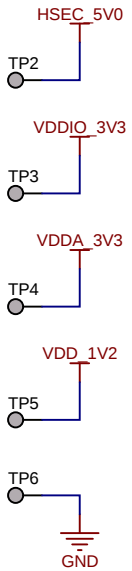
C

C

D

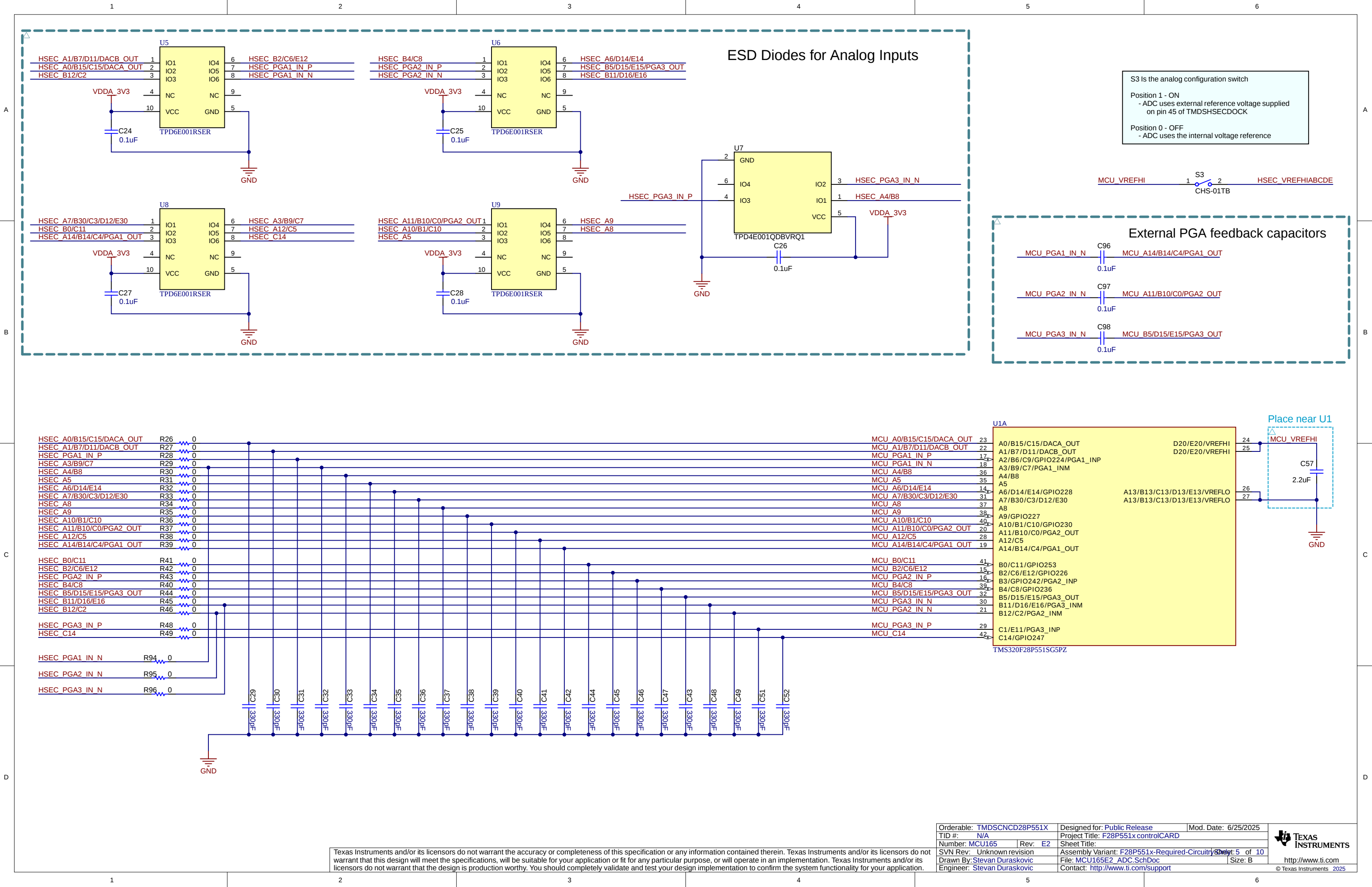
D

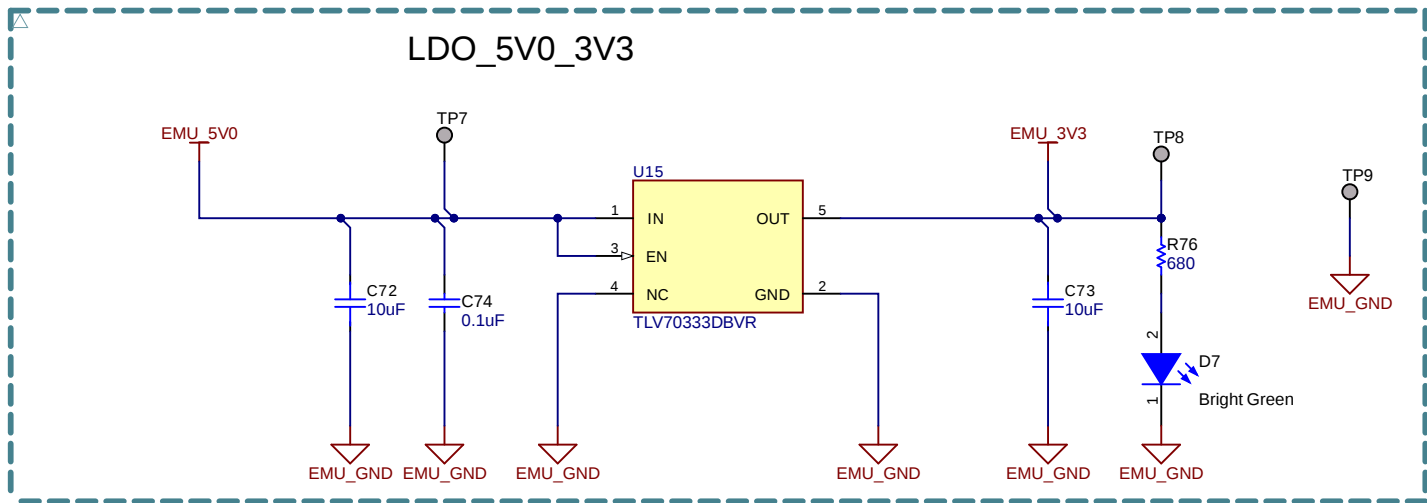
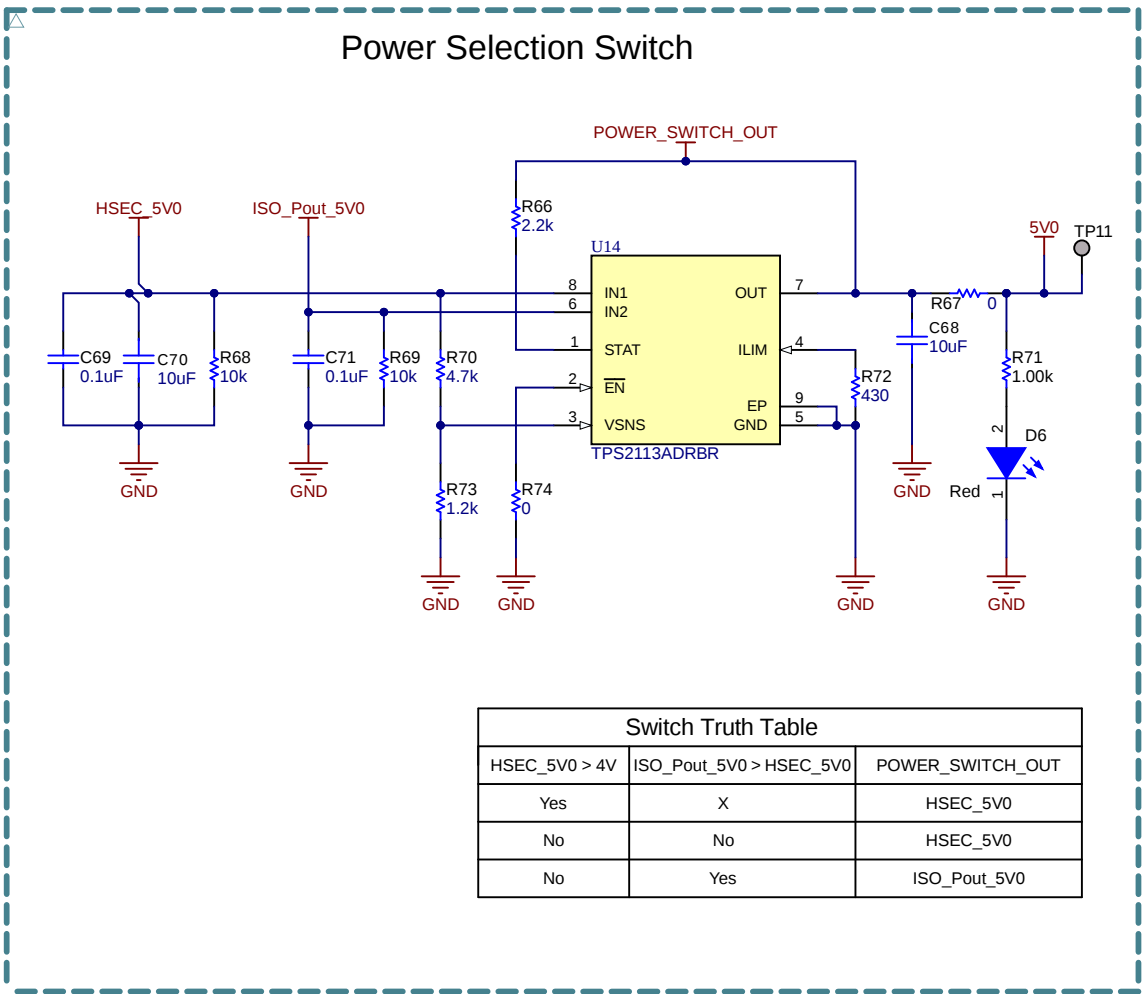
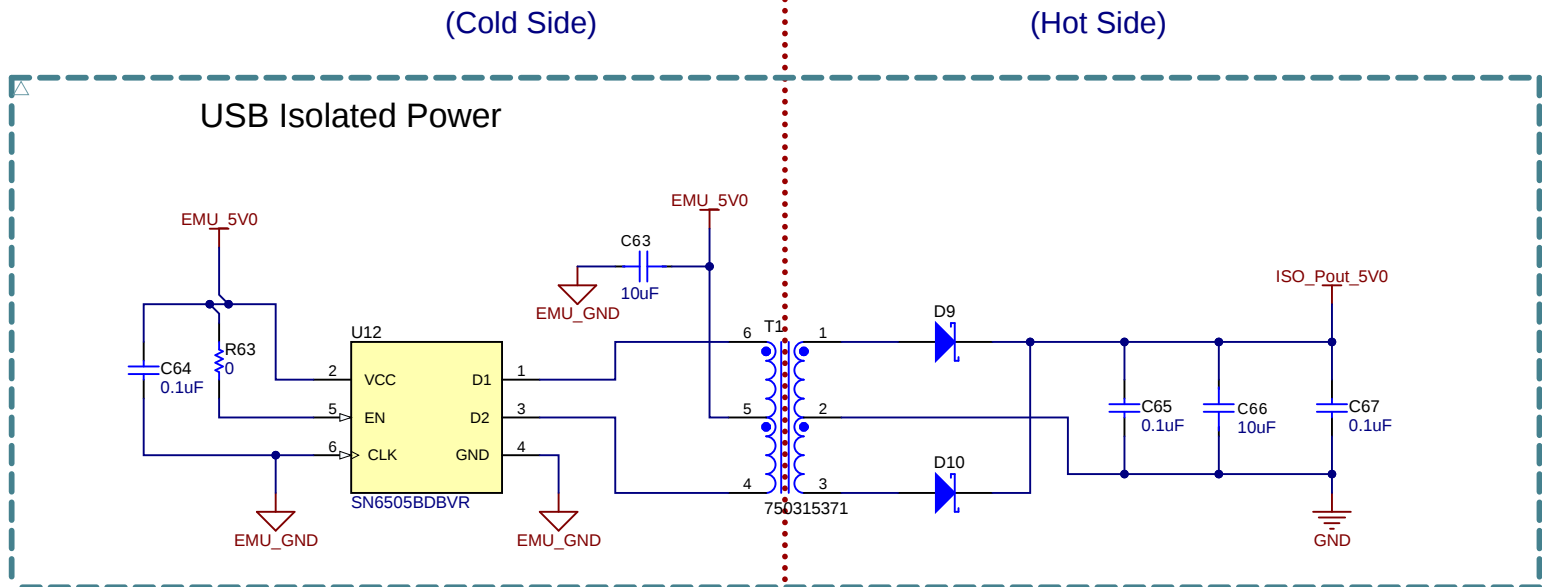
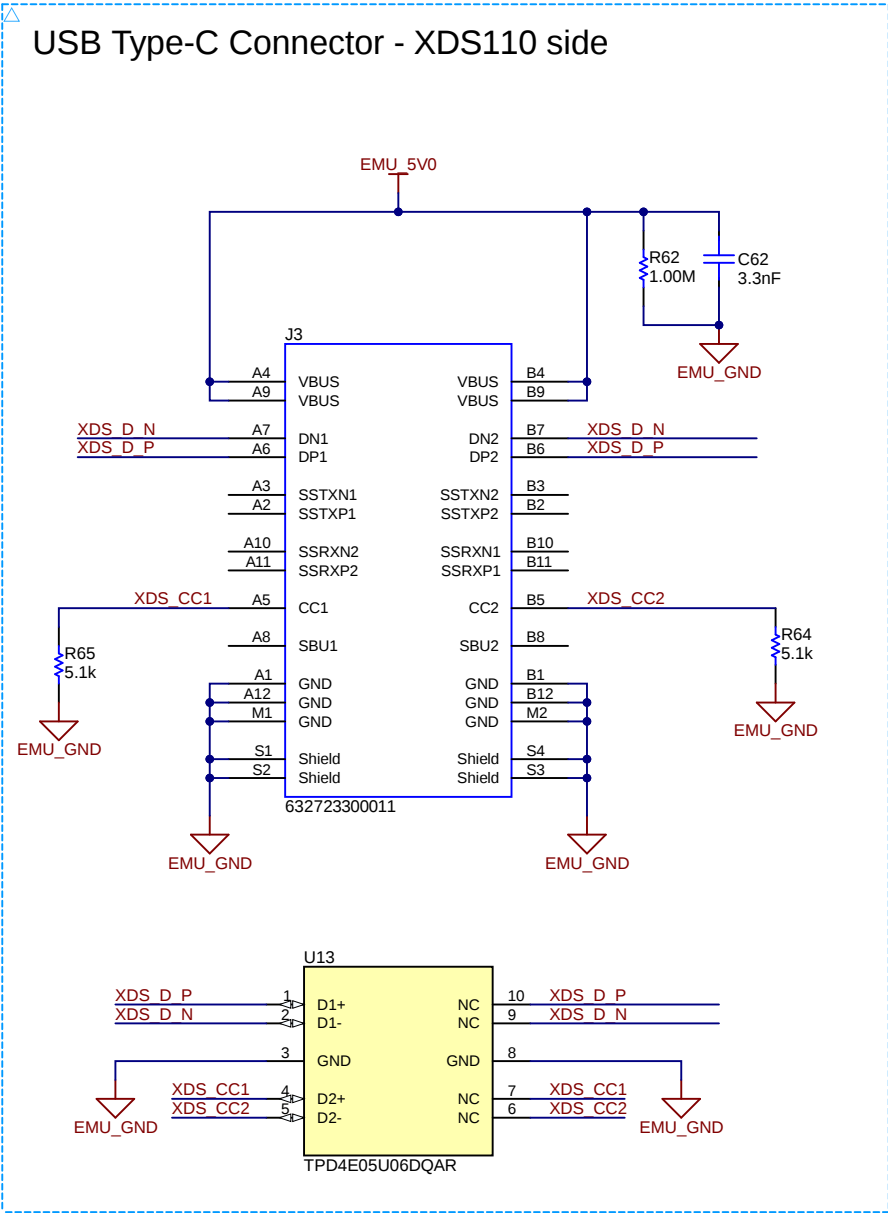


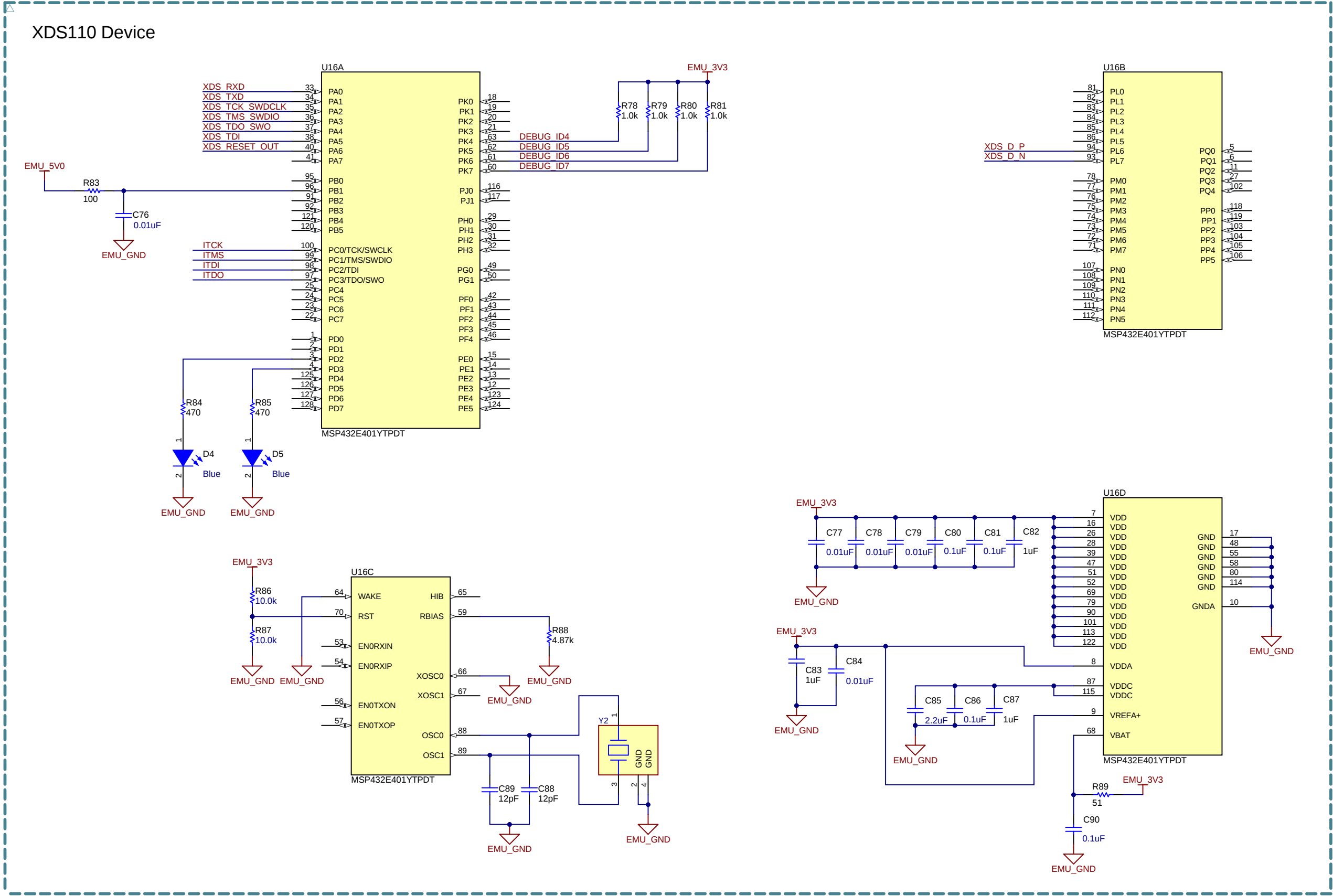


The F28P551x controlCARD uses the internal VREG to generate the 1.25V voltage rail for VDD.

For custom boards using external VREG mode, recommend to use LDO (e.g., TPS745-Q1) to generate both 3.3V and 1.25V supplies.







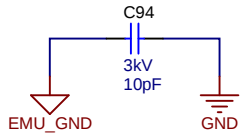
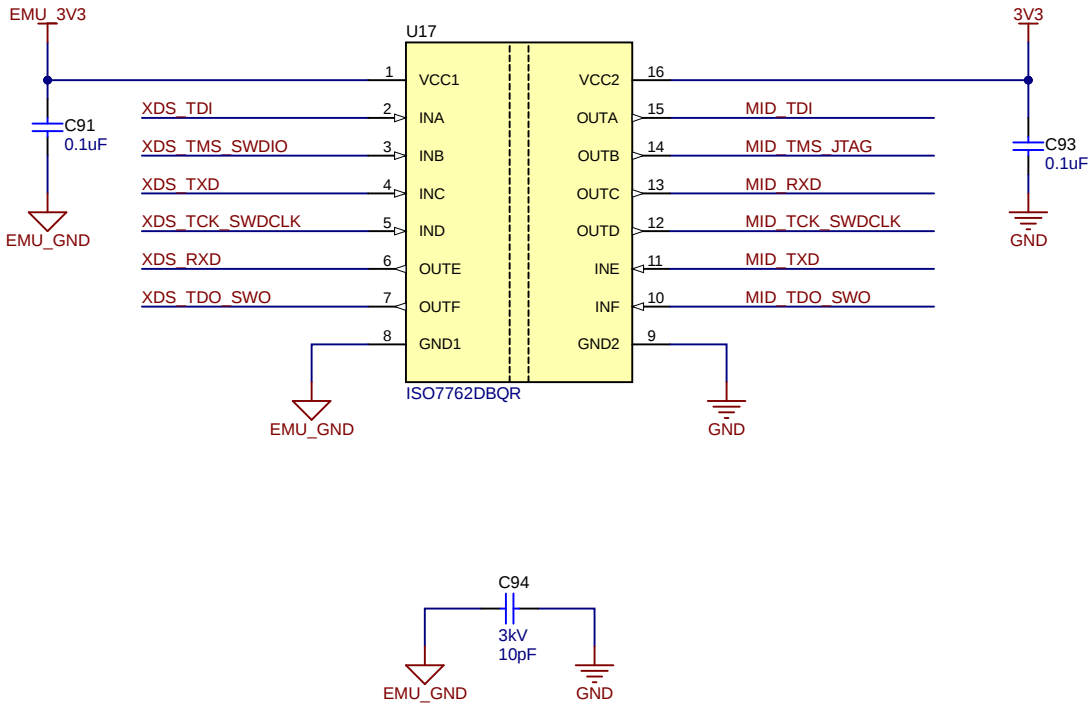
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Orderable: TMDSCNCD28P551X	Designed for: Public Release	Mod. Date: 6/25/2025
TID #: N/A	Project Title: F28P551x controlCARD	
Number: MCU165	Rev: E2	Sheet Title:
SVN Rev: Unknown revision	Assembly Variant: F28P551x-Required-Circuitry	Sheet 8 of 10
Drawn By: Stevan Duraskovic	File: MCU165E2_XDS110_MCU.SchDoc	Size: B
Engineer: Stevan Duraskovic	Contact: http://www.ti.com/support	

NOTE: Because the JTAG signals are isolated, cJTAG is not supported on this controlCARD.

(Cold Side)

(Hot Side)



WARNING: To avoid potential shock hazard in high-voltage settings, leave the Y cap (C94) unpopulated from the EVM.

S4 - JTAG Emulation & UART Switch

POS 1 ON: Use XDS110 emulator that is on the cCARD
POS 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
POS 2 ON: GPIOs 28 & 29 will be connected to the USB-to-UART adapter on the XDS110 emulator
POS 2 OFF: GPIOs 28 & 29 are disconnected from the USB-to-UART adapter on the XDS110 emulator and connected to the HSEC connector pins

